AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. – 3. (cancelled)

4. (previously presented) A manufacturing method for a semiconductor device comprising:

a hole portion formation step for forming hole portions whose entire width is substantially identical to the width of the opening portion in a part of the active surface side of the substrate on which electronic components are formed;

a curved surface formation step for curving the bottom surface of the hole portion while maintaining the width of the bottom surface in the hole portions substantially identical to the width of the opening portion;

a connecting terminal formation step for forming connecting terminals that serve as the external electrodes of the electronic circuits by burying metal in the hole portions;

an exposure step for exposing a part of the connecting terminals by carrying out processing on the back surface of the substrate; and

an insulating film formation step of forming an insulating film on the inner wall and the bottom surface of the hole portions between the curved surface formation step and the connecting terminal formation step, and further

the exposure step comprising:

a first etching step for etching the back surface of the substrate until the thickness of the substrate is approximately slightly thicker than the burying depth of the connecting terminals;

a second etching step for exposing the insulating film formed in the hole portions by etching the back surface of the substrate at an etching rate that is lower than the etching rate in the first etching step; and

a third etching step for exposing the connecting terminals by etching at least a part of the exposed insulating film.

5. – 6. (cancelled)

7. (previously presented) A manufacturing method for a semiconductor device comprising:

a concavo-convex shape formation step for forming a concavo-convex shape on a part of the active surface side of the substrate on which the electronic circuits are formed;

a hole formation step for forming hole portions by etching the area in which the concavo-convex shape has been formed, whose entire width is substantially equal to the width of the area on which the concavo-convex shape has been formed and whose bottom surface has a shape substantially identical to the concavo-convex shape;

a connecting terminal formation step for forming the connecting terminals that serve as the external electrodes of the electronic circuits by burying metal in the hole portions;

an exposure step for exposing a part of the connecting terminals by carrying out processing of the back surface of the substrate; and

an insulating film formation step for forming an insulating film on the inner wall and the bottom surface of the hole portions between the hole formation step and the connecting terminal formation step, and further

the exposure step comprising:

a first etching step for etching the back surface of the substrate until the thickness of the substrate is approximately slightly thicker than the burying depth of the connecting terminals;

a second etching step for exposing the insulating film formed in the hole portions by etching the back surface of the substrate at an etching rate that is lower than the etching rate in the first etching step; and

a third etching step for exposing the connecting terminals by etching at least a part of the exposed insulating film.

8. – 9. (cancelled)

10. (previously presented) A manufacturing method for a semiconductor device comprising:

a mask formation step for forming a mask having a plurality of holes in the hole formation area set in a part of the active surface side of the substrate on which the electronic circuits are formed;

a concavo-convex shape hole formation step for forming hole portions whose entire width is substantially identical to the width of the hole formation area and whose bottom surface has a concavo-convex shape by etching the substrate through each of the holes formed in the mask using an etching method in which the holes widen slightly in the surface direction of the substrate;

a connecting terminal formation step for forming connecting terminals that serve as the external electrodes for the electronic circuits by burying metal in the hole portions;

an exposure step for exposing a part of the connecting terminals by carrying our processing on the back surface of the substrate; and

an insulating film formation step for forming an insulating film on the inner wall and the bottom surface of the hole portions between the concavo-convex hole formation step and the connecting terminal formation step, and further

the exposure step comprising:

a first etching step for etching the back surface of the substrate until the thickness of the substrate is approximately slightly thicker than the burying depth of the connecting terminals;

a second etching step for exposing the insulating film formed in the hole portions by etching the back surface of the substrate at an etching rate that is lower than the etching rate in the first etching step; and

a third etching step for exposing the connecting terminals by etching at least a part of the exposed insulating film.

11. – 31. (cancelled)